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A SPICE Model for the Gate Current of HEMT's

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Abstract

A model for simulating the DC characteristics of the gate junction in High Electron Mobility Transistors is presented. The equations for the gate current of FET's in the SPICE simulator are modified to account of the HEMT gate current in a wide range of bias conditions. It is proven that a four-diodes model yields to a satisfactory agreement with the experimental data. The presented model can be employed either by implementing the modified equations in the simulator code or by a device macro modeling.

I. Introduction

High Electron Mobility Transistors (HEMT's) are widely used for analog as for digital circuits. Models of HEMT's for circuit simulators have been developed accounting essentially for the device drain characteristics [1-3]. Studies about the HEMT's gate junction have been performed but were restricted to particular bias conditions of the device [4-8]. We have investigated the I-V characteristics of the gate-channel junction of HEMT's in a wide range of operative bias conditions. We have found that the SPICE model of FET's is completely inadeguate to reproduce the experimental data. The necessity of an adequate model accounting for the gate current is enhanced in the design of circuits in which the gate electrode is loaded by a relatively high impedance, or if the DC gate current can significantly charge a capacitance [9]. In HEMT's digital circuits the gate current can affect logic swing and noise margins [10, 11]. Moreover, an accurate modeling of the gate characteristics is useful for analog circuits whose performance are influenced by the noise associated with the gate current [12, 13].

In this work we present a model directly implementable in circuit simulators and reproducing the experimental HEMT's gate current characteristics in a wide range of biasing conditions.

II. Experimental

The following analysis starts by testing enhancement type HEMT's made in Fraunhofer Institut for Applied Solid State Physics (Freiburg, Germany). The HEMT's are double δ-doped with a gate length and width of 0.3 μm and 50 μm, respectively [14, 15]. The gate current has been measured using a HP4145 voltage source-electrometer. In Fig. 1 the absolute value of the gate current of an enhancement-type HEMT is shown as a function of V_{GS}, with V_{DS} as parameter. Differently from silicon FET's, it results that the HEMT's gate current strongly depends on the bias point of the transistor. It is observed that for V_{GS}=0 and V_{DS}>0 the measured current is negative (it flows out of the gate) while, as the gate voltage is increased above particular V_{GS} values, dependent on V_{DS}, the gate current changes sign (it flows into the gate). It results that, for each characteristic curve, a point at which the measured current is practically zero exists (represented by the minimum in the logarithmic scale of Fig. 1).

The observed behaviour can be explained by considering that the gate current is the sum of two

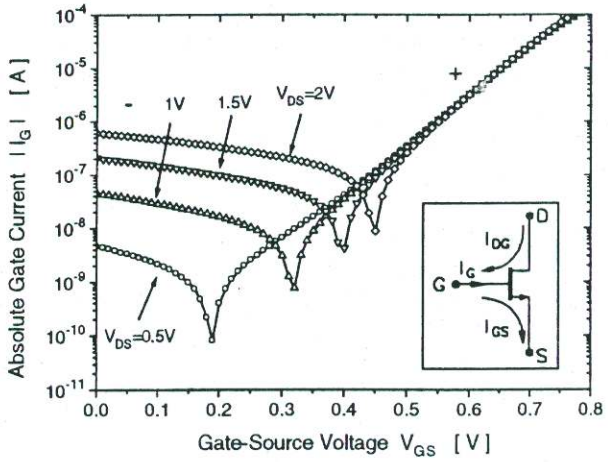

Fig. 1 Experimental I-V characteristics of the gate-channel junction of an enhancement type HEMT with V_{DS} as parameter. The absolute value of the gate current is represented and the sign of the current is indicated (positive if it enters into the gate). The observed characteristics can be explained if the gate current is assumed to be constituted by two components I_{GS} and I_{DG} (inset) positive when indicated as in the picture.

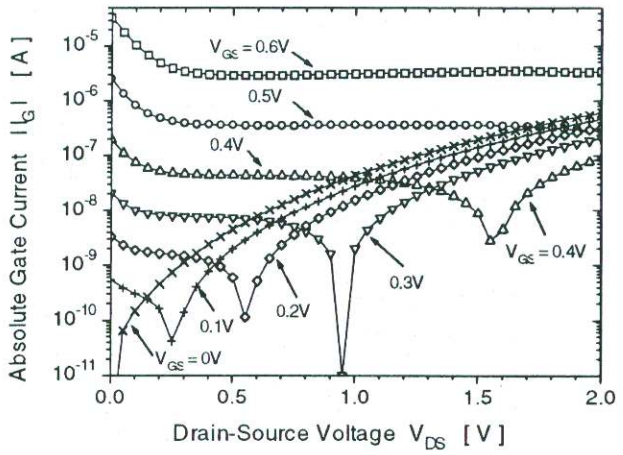

Fig. 2 Experimental I_G vs V_{DS} characteristics of the gate-channel junction of an enhancement type HEMT with V_{GS} as parameter.

components as represented in the inset of Fig. 1. We can assume that the current I_{GS} mainly depends on V_{GS} and it is positive when the gate-channel junction is forward biased, as normally is for enhancement-type HEMT's. The other component, I_{DG} , can be positive or negative depending on the drain-gate bias. When $V_{DG} > 0$, the current $I_{DG} > 0$ flows through that part of the gate-channel junction which is reverse biased. It can be assumed that I_{DG} depends mainly on the potential difference between the gate and the drain and increases as V_{DG} increases. The minimum in the measured gate current I_G (Fig. 1) can be explained as corresponding to the bias condition in which the two components are equal, so that I_G=0.

In Fig. 2 the measured gate current is reported as a function of V_{DS} with V_{GS} as parameter. These curves can be directly associated with the I_D-V_{DS} characteristics of the transistor. Also this graph can be easily explained in terms of the two mentioned components of the gate current. In particular the flat part of the characteristics for $V_{GS} \geq 0.4$V corresponds to the situation in which $I_{GS} >> I_{DG}$ so that $I_G \approx I_{GS}$ does not depend significantly on V_{DS}. In Fig. 2 it can be also noted a relevant increase in I_G when V_{DS} decreases below 0.2 V. This behaviour can be qualitatively explained with the simple model of Fig. 1. In fact, at V_{DS}=0 the transistor actually behaves as a diode with the whole gate-channel junction forward biased, so that $I_{GS} > 0$ and $I_{DG} < 0$ have the same direction. As soon as V_{DS} is sligtly increased above 0 V, a part of the gate-channel junction at the drain end of the gate becomes less forward biased and does no more contribute significantly to the total gate current, so that a sharp drop in I_G is observed. This phenomena can be better understood thinking to the distributed nature of the gate junction, having a forward biased part whose area is a function of V_{DG}. Also in the characteristics of Fig. 2, minimums of $|I_G|$ are observed, for which $I_{GS} \approx I_{DG}$. At the left side of each minimum, I_{GS} is the dominant component, while at the right side $I_G \approx I_{DG} < 0$.

II. The Model

In the standard SPICE model for FET's the gate-channel junction is described by two diodes connecting the gate with source and drain as shown in Fig. 3A. The gate current is calculated using the following equation [16]

$$I_G = I_{GS} - I_{DG} = I_S\left(e^{V_{GS}/NV_t} - 1\right) + I_S\left(e^{V_{GD}/NV_t} - 1\right) \quad (1)$$

in which I_S, N and V_t are the saturation current, the emission coefficient (also called 'ideality factor') and the thermal voltage, respectively. It is easily verified that this model can not describe the experimental gate characteristics of HEMT's. In fact the reverse current of each diode is supposed to be constant (=-I_S) so that the dependence of the HEMT gate current by the drain-source voltage is not reproduced.

In order to synthesize a model, it can be observed that the current I_{DG} of the reverse biased gate-drain junction has a quasi-exponential dependence on V_{DG} (see Fig. 2 at V_{GS}=0). Taking this into account the characteristics of Fig. 1 can be also quantitatively justified because the gate current results to be the difference of two currents, I_{GS} and I_{DG} , of the same order of magnitude and both having a quasi exponential dependence on the related voltages, V_{GS} and V_{DG} respectively. The basic observation, derived by the experimental data, is that the gate-channel junction at the drain end, when reverse biased, shows a characteristic similar to a forward biased junction.

We found that the observed gate characteristics can be modelled by a four-diodes model, represented in Fig. 3B and described by the following three equations

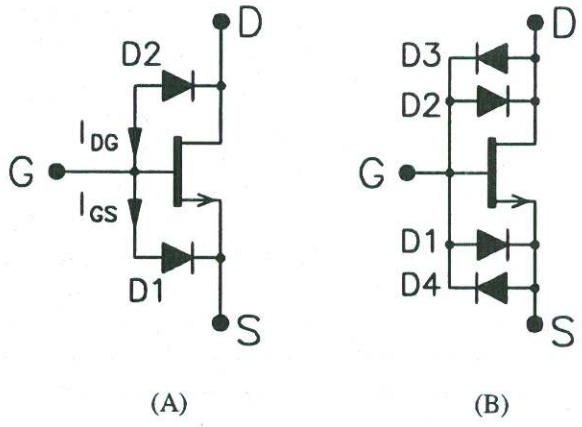

Fig. 3 (A) GaAs FET model implemented in SPICE. The gate-channel junction is modelled with the two diodes D1, D2. (B) The new proposed four diodes model.

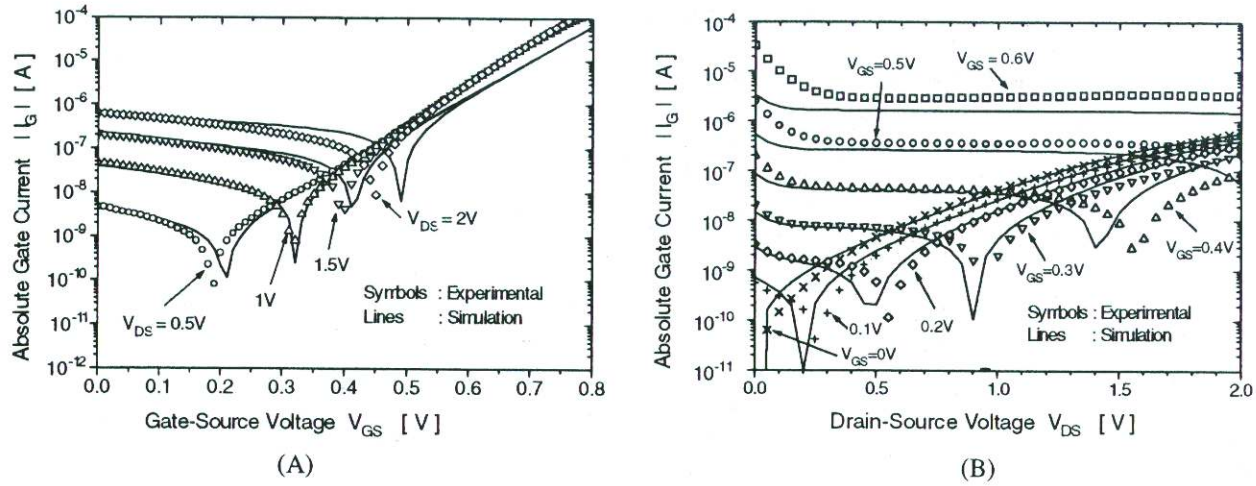

Fig. 4 Comparison between the model and the experimental I-V characteristics of the gate junction of an enhancement type HEMT. The absolute value of the gate current is reported (A) as function of V_{GS} with V_{DS} as parameter, (B): as function of V_{DS} with V_{GS} as parameter.

$$I_{GS} = I_{S1}\left(e^{V'_{GS}/N_1V_t} - 1\right) - I_{S4}\left(e^{-V'_{GS}/N_4V_t} - 1\right) \quad (2a)$$

$$I_{DG} = -I_{S2}\left(e^{V'_{GD}/N_2V_t} - 1\right) + I_{S3}\left(e^{-V'_{GD}/N_3V_t} - 1\right) \quad (2b)$$

$$I_G = I_{GS} - I_{DG} \quad (2c)$$

The first term in (2a) and (2b) accounts for the characteristics of the diodes D1 and D2 while the second terms for the characteristics of the diodes D3 and D4. The diode model includes also a series resistance which is necessary for taking into account for the non-perfect exponential characteristic: the apexes on V'_{GS} and V'_{GD} indicates the true voltage across the ideal junction. For each diode three parameters (I_S, N, R) have to be determined. If the device can be assumed symmetrical with respect to the source and drain, the diodes D1 and D2 can be taken identical, as for D3 and D4, reducing the number of the free parameters to six. This model can be employed either by implementing the modified equations in the simulator code or by using a device macro model as indicated in Fig. 3B.

Fitting parameters	Value
$N_1=N_2$	2.18
$I_{S1}=I_{S2}$	28 pA
$R_1=R_2$	0 Ω
$N_3=N_4$	9.22
$I_{S3}=I_{S4}$	5.9 nA
$R_3=R_4$	73 kΩ

Table I. Fitting parameters for the diodes of the model as calculated from a least square fitting of the experimental data.

III. Test of the Model

The model has been compared with the experimental data presented in Sect. I. The extraction of the model parameters has been done using a least square fitting automatic procedure to the experimental characteristics. The modeled HEMT is symmetric so that D1 and D2 are taken identical, as also D3 and D4. The parameters of D1 (I_{S1}, N_1, R_1) have been derived by one of the experimental characteristics $\log(|I_G|)$ vs. V_{GS} (Fig. 1) in strong forward biased condition (for example: V_{DS}=0.5V and V_{GS}>0.3V) for which $I_G \approx I_{GS}$ is practically due to D1. The parameters for D3 (I_{S3}, N_3, R_3) have been extracted by the characteristic $\log(|I_G|)$ vs. V_{DS} with V_{GS}=0 (Fig. 2), so that $I_G \approx -I_{DG}$ is due to D3. The values of the extracted parameters are reported in Table I.

The comparison between the model and the experimental data for the enhancement-type HEMT is shown in Fig. 4 A and B. At V_{GS} values higher that 0.5V (Fig. 4A) an increase of the slope of the characteristics and a displacement of the model from the experimental data are observed. This phenomena is not clear and could be probably related to the device heating. This effect also shift toward lower V_{GS} the point at which the minimum $|I_G|$ is measured.

In Fig. 4B the comparision between the experimental and the model data for the $|I_G|$ vs V_{DS} characteristics is shown. The agreement is in general quite satisfactory. The stronger increase of the experimental gate current as V_{DS} approaches 0V is due to the distributed nature of the gate-channel junction, as qualitatively explained in Sect. II. A analytical model accounting for this effect has been done by Ruden et al. [6]. An accurate modeling of this part of the characteristic could be also done with the proposed four diodes model by taking the diode D1 active area as a decreasing function of V_{DG}. This generally

requires the possibility to change the equation set of the diode in the simulator code.

It is worthwhile to note the relatively high value of the series resistance R_3 of the D3 diode, which is necessary to describe the non perfect exponential I_{DG}-V_{DG} characteristic (see Fig. 4B for V_{GS}=0). It should be remembered that R_3 is not a physical resistor and so its thermal noise source must be disactivated during a noise simulation. This is a non standard option and requires modifications in the simulator code.

IV Summary and Perspectives

The experimental HEMT's gate characteristics can be explained in a wide range of bias conditions by considering two current components, one dependent mainly on V_{GS} and the other on V_{DG} voltage. A model for the gate current suitable for circuit's simulators, as SPICE, has been proposed, describing the gate-channel junction by means of four diodes. The model for a symmetrica device makes use of six parameters which can be easily extracted by the experimental data. A satisfactory agreement with the experimental behaviour is found for enhancement-type HEMT's.

Since the behaviour of the gate current in enhancement type HEMT's can be also observed in depletion type HEMT's and in MESFET's, this model could be adapted also to this type of transitors.

An even more accurate description of the gate characteristics can be done by implementing in the simulator the distributed nature of the gate-channel junction and by investigating the dependence of the parameters on the temperature.

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